FIELD EFFECT TRANSISTOR, UJT, SCR, TRIAC

SCOPE OF THE CHAPTER

This chapter introduces another type of transistor family known as Field Effect Transistor. It includes construction, working and characteristics of junction field effect transistor (JFET) and metal oxide semiconductor field effect transistor (MOSFET).

Also this chapter introduces the new semiconductor devices namely unijunction transistor (UJT) silicon controlled rectifier (SCR) and TRIAC along with their construction, working and VI characteristics.

INTRODUCTION

Already we have discussed about the BJT in which both holes and electrons play part in the conduction process. Hence its name is bipolar junction transistor. But BJT has two main disadvantages.
1) It has low input impedance because of forward biased emitter- base junction.
2) It has considerable noise level.

These two disadvantages of BJT are overcome in field effect transistor, which offers high input impedance and minimum noise level.
We know that BJT is the current controlled device as the output characteristics are controlled by input current. FETs are the voltage controlled device i.e. its output characteristics are controlled by input voltage.
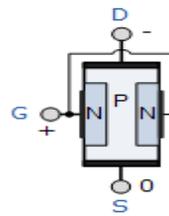
Basically there are two types of FETs.
1) Junction Field Effect Transistor (JFET)
2) Metal Oxide Semiconductor Field Effect Transistor (MOSFET)
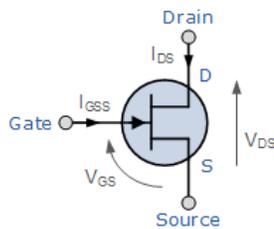
STRUCTURE OF JFET

A JFET is a three terminal semiconductor device in which current conduction is by one type of carriers i.e. by holes or electrons.

Construction –
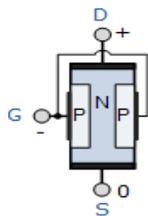
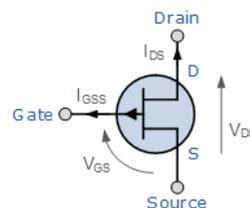N-channel JFET   P-channel JFET
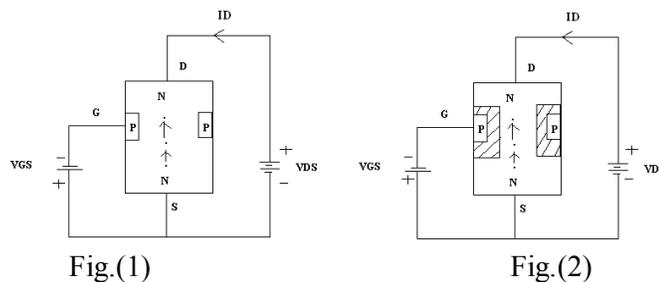

N-channel JFET   P-channel JFET

JFET consists of a p-type or n-type silicon bar containing two pn –junctions at the side as shown in the figure above. If the bar is n-type then it is called as n-channel JFET and if the bar is p-type then it is called as p-channel JFET.

In the construction of n-channel JFET a narrow bar of n-type semiconductor is taken and two p-type regions are defused on the opposite sides of middle part. This forms two pn-junction diodes. These two heavily doped p-regions are internally connected and a common terminal is taken out which is known as gate terminal.

The ohmic contacts are me to the two ends of the bar. One lead is called as the source terminal and the other is called as drain terminal. A source is a terminal through which majority carriers enter the bar and drain is the terminal through which they leave the bar. Thus FET has three terminals- gate, source and drain.

For normal operation of JFET, the voltage between the gate and source is such that the gate is reverse biased.

OPERATION OF N-CHANNEL JFET

Fig.(1)   Fig.(2)

The above figure shows the circuit for n-channel JFET with normal polarities i.e. gate is reverse biased. The circuit operation takes place as follows.

1) When voltage V_{DS} is applied between drain and source and if $V_{GS} = 0$, then the two pn-junctions at the sides of the bar establishes depletion layers. The electrons will flow from source to drain through a channel between the depletion layers. The size of these layers determines the width of the channel and hence the current conduction through the bar.

2) When the reverse voltage V_{GS} is applied between the gate and source, the width of the depletion layer is increased. This reduces the width of the channel and hence current flowing through the channel reduces. If reverse voltage on the gate is decreased, the width of the depletion layer also decreases resulting in the increase width of conducting channel. Hence the current flowing through the channel increases.

3) If the reverse voltage applied at gate terminal is increased then the depletion layers are able to touch each other due to which the channel is pinched off i.e. fully blocked due to which the current flowing through the channel becomes zero. The value of this reverse voltage V_{GS} at which the drain current becomes zero is known as V_{GS} (off).

From the above discussion it is clear that, the current flowing through the device is controlled by the input voltage V_{GS} and hence this is known as voltage controlled device or Field Effect Transistor.

It may be noted that the p-channel JFET also works in the same manner except that channel current carriers will be the holes instead of electrons.

OUTPUT CHARACTERISTICS OF JFET The output characteristics are shown in fig (3) which can be defined as the graph between the output current I_D and output voltage V_{DS} keeping input voltage V_{GS} constant. The different curves for different values of V_{GS} are shown in the fig (3). From the graph the following points can be noted. In order to explain typical shape of output characteristics, we select the curve with $V_{GS} = 0$ which is subdivided in the following regions.

1) Ohmic region
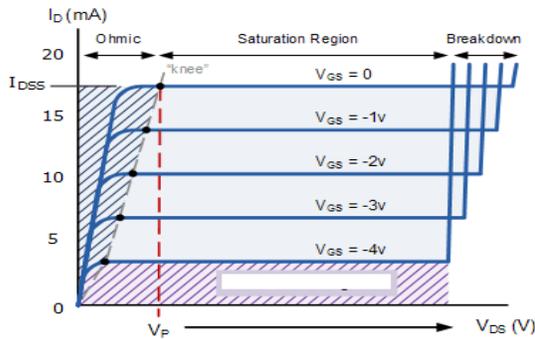
If the gate is shorted with source, the maximum drain current flows through the channel which is denoted as I_{DSS} and known as shorted gate drain current. This region is shown as a curve OA in the figure. In this region the drain current I_D increases linearly with the increase in drain to source voltage V_{DS} obeying Ohm's law. This linear characteristic is due to the fact that the n-type semiconductor bar acts like simple resister.

2) Curve AB (Saturation region)

At point A the drain current almost becomes constant this value of V_{DS} above which the I_D becomes constant is called as pinch off voltage V_P. After pinch of voltage the channel width becomes so narrow that the depletion layers almost touch each other. The drain current passed through the small passage between these layers and hence increase in drain current is very small with V_{DS} above pinch of voltage V_P. Consequently drain current I_D remains constant. This region where I_D is constant is known as Active region, where JFET works as a constant current source.

3) Breakdown region

If the maximum drain voltage $V_{DS\ (max)}$ is applied to JFET then the drain current sharply increases resulting in the breakdown of JFET. Hence the region above $V_{DS\ (max)}$ is known as breakdown region. Hence the voltage applied to drain should be less than $V_{DS\ (max)}$ for safety purpose.

Transfer characteristic:

The graph between the drain current I_D and V_{GS} is called as transfer characteristics of JFET. From the below graph it is clear that I_D is maximum when $V_{GS} = 0$ and I_D is zero for maximum reverse value of V_{GS}.

JFET parameters

JFET has certain parameters which determine its performance in a circuit which are as follows.

1) a.c. drain resistance (r_d)

It is also called as dynamic drain resistance and defined as the ratio of change in drain to source voltage (ΔV_{DS}) to the change in drain current (ΔI_D) at constant gate to source voltage V_{GS}.

$$r_d = \Delta V_{DS} / \Delta I_D \text{ at constant } V_{GS.}$$

2) Trans conductance (g_m)

It is defined as the ratio of change in drain current ΔI_D to the change in gate to source voltage ΔV_{GS} at constant drain to source voltage $V_{DS.}$

$$g_m = \Delta I_D / \Delta V_{GS} \text{ at constant } V_{DS}$$

3) Amplification factor (μ)

It is defined as the ratio of change in drain to source voltage (ΔV_{DS}) with respect to change in gate to source voltage ΔV_{GS} keeping I_D constant.

$$\mu = \Delta V_{DS} / \Delta V_{GS} \text{ at constant } I_D$$

Relation between μ, g_m and r_d : We know that $\mu = \Delta V_{DS} / \Delta V_{GS}$
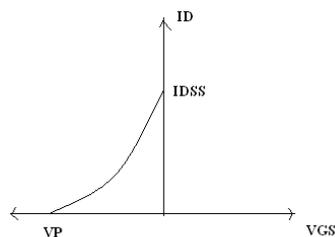

Fig. Transfer characteristics of FET

Dividing numerator and denominator of R.H.S by ΔI_D we get

$$\mu = (\Delta V_{DS} / \Delta V_{GS}) * (\Delta I_D / \Delta I_D)$$

$$\mu = (\Delta V_{DS} / \Delta I_D) * (\Delta I_D / \Delta V_{GS})$$

$$\mu = r_d * g_m$$

Metal Oxide Semiconductor Field Effect Transistor (MOSFET):-

MOSFET is an important semiconductor device and widely used in many applications. The input impedance of MOSFET is much more than that of JFET because of very small gate leakage current. There are two types of MOSFETs – Depletion MOSFET and Enhancement MOSFET.
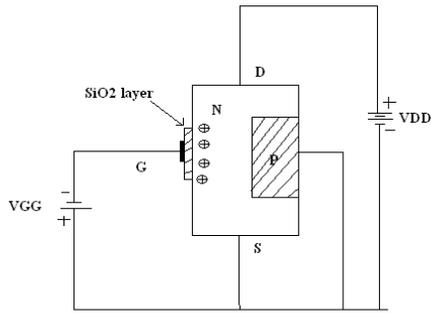
1) Depletion MOSFET:-

The following figures show the construction details and symbol of Depletion MOSFET. It consists of conducting bar of N-type material with an insulated gate on the left and p-type region on the right side.

Free electrons can flow from source to drain through N-type bar. The p-region is called substrate. A thin layer of SiO_2 is deposited on left side of the channel, which insulates the gate from the channel.

Fig. Construction and working of depletion MOSFET

n-chanel MOSFET   p-chanel MOSFET
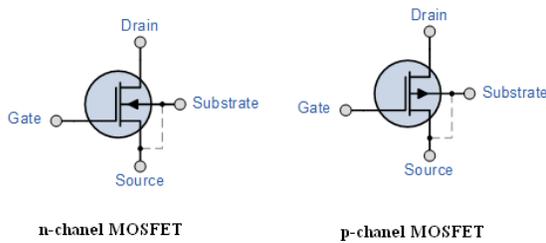
The basic construction of p-channel MOSFET is similar to n-channel MOSFET except that conducting bar is of p-type material and substrate is of n-type material.

Working

The working of MOSFET may be explained easily if we visualize the entire structure of the device as a parallel plate capacitor.

The negative voltage on the gate induces a positive charge in the channel. Because of these free electrons in the vicinity of positive charge are repelled away in the channel. As a result of this the channel is depleted of free electrons. This reduces the no. of free electrons which reduces the drain current passing through the channel. Therefore if larger the value of V_{GS} then smaller the values I_D. When the $V_{GS} = - V_P$ then $I_D = 0$. On the other hand conductivity of n-channel increases for positive value of V_{GS} as shown in the figure below.
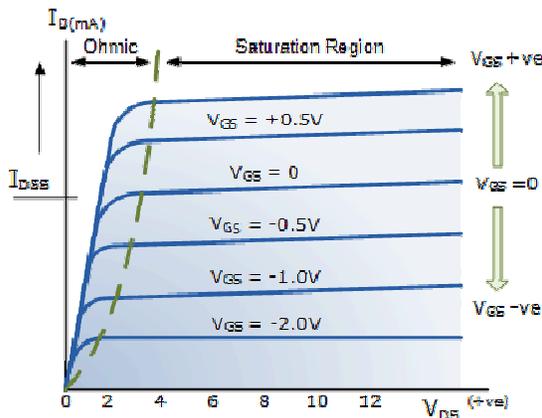
2) Enhancement MOSFET:–

The figure below shows symbol of n-channel and p-channel Enhancement MOSFETs. It consist of a supporting P region called as substrate, which has two broad n^+ material regions forming drain (D) and source (S). The n^+ region means a region which is heavily doped.
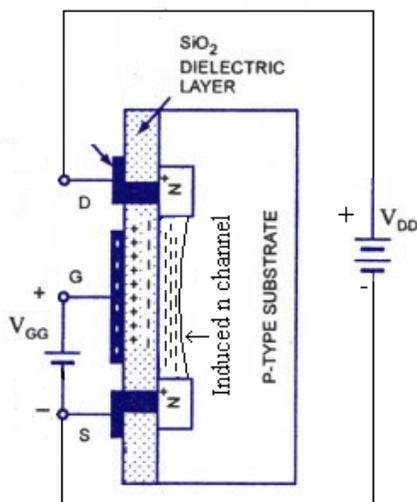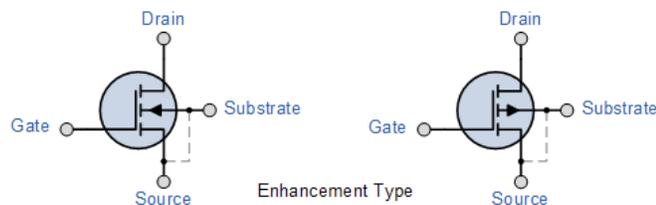
Fig.1 Structure

Enhancement Type

This MOSFET is always operated with the positive gate to source voltage V_{GS}. There is no drain current for $V_{GS} = 0$. Therefore Enhancement MOSFET is also called normally off MOSFET.

If some positive voltage is applied at the gate it induces a negative charge in p-type substrate just adjacent to SiO_2. The induced negative charge is produced by attracting the free electrons from the source. When the gate is positive enough it can attract a no. of free electrons. This forms a thin layer of electrons, which
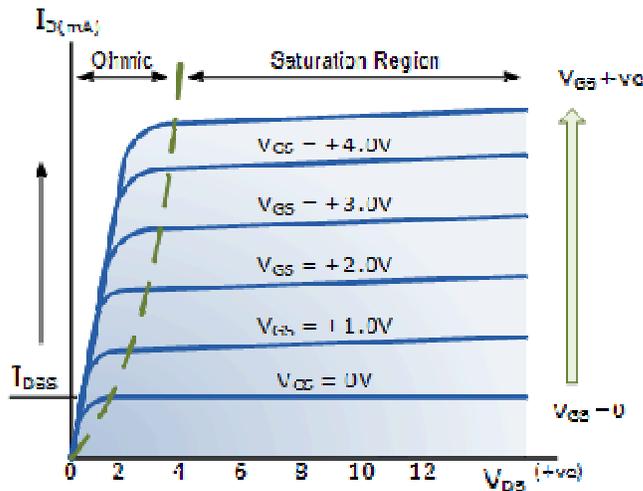
stretches from source to drain. This effect is equivalent to producing a thin layer of n-type channel in p-type substrate. This layer of free electrons is called n-type inversion layer. The minimum gate to source voltage V_{GS}, which produces inversion layer is called threshold voltage $V_{GS\,(Th)}$.

Figure below shows characteristics of n-channel enhancement MOSFET

Applications of MOSFET

1) It is used as buffer amplifier
2) In low noise amplifier.
3) Large scale integrate circuits for microprocessors, memory devices etc.
4) In cascaded amplifiers
5) In sample and hold circuits which are used in analog to digital convertors.

Advantages of MOSFET over JFET

1) They are easier to manufacture.
2) They are smaller in size.
3) Capacitive effects are lower and input resistance is higher.
4) They can operate in depletion and enhancement mode, while JFETs operate only in depletion mode.

UNIJUNCTION TRANSISTOR (UJT)

A Unijunction transistor is a three terminal semiconductor device having only one p-n junction like diode but has three terminals. This device has a unique characteristics that when it is triggered, the emitter current increases regeneratively until is limited by emitter power supply. The unijunction transistor can be employed in a variety of applications like switching pulse generator, saw tooth generator etc. The basic construction of UJT and its symbol is shown in below figure.
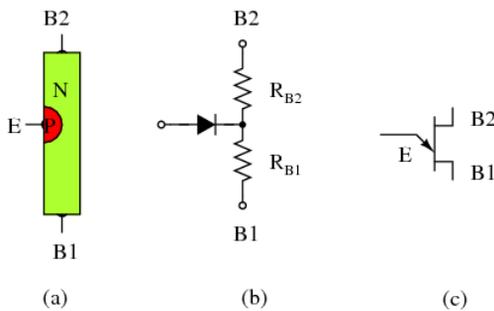
It consists of an N type silicon bar with an electrical connection on each end and the leads to these connections are called base leads, Base 1 (B1), Base 2 (B2). The small p-type region is doped at one side of the bar near to B2 terminal and the lead taken from this p-type region is known as emitter. Thus a p-n junction is formed between the emitter and base region. The emitter region is heavily doped, while the base region is lightly doped. So resistivity of base material is very high.

The resistance ratio is an important characteristic of UJT which is known as intrinsic stand-off ratio which is denoted by **η** which is given by the equation

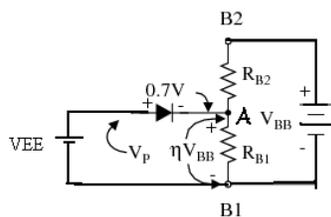$$\eta = \frac{R_{B1}}{R_{B1} + R_{B2}}$$
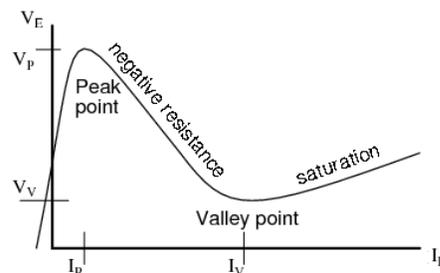
Operation

Fig.1 Circuit arrangement

Fig.2 Characteristic

Here emitter diode is reverse biased by voltage drop across resistance R_{B1} and its own barrier potential V_D. So total reverse bias is $V_D + V_B = V_D + \eta\, V_{BB}$ (for silicon $V_D = 0.7$ Volts). As long as applied emitter voltage is below the total reverse bias voltage across the diode, it remain reverse biased. And there is no emitter current. The value of emitter voltage which causes the diode conduction is called peak point voltage V_P.

i.e. $V_P = \eta V_{BB} + V_D$.

Then the UJT is turned on and emitter current begins to flow. Under this condition the UJT is said to be fired or triggered or turned on.

Thus as V_E along with I_E increases, R_{B1}, η and V_A decreases. This produce further decrease in R_{B1}, η and V_A. This process is regenerative. V_A as well as V_E decreases as I_E increases. Due to this the UJT has negative resistance region in its VI characteristics.

The curve between Emitter voltage V_E and emitter current I_E of a UJT at a given voltage V_{BB} between the bases this is known as emitter characteristics of UJT

Initially in the cut off region as V_E increases from zero, slight leakage current flows from terminal B2 to the emitter the current is due to the minority carriers in the reverse biased diode.

Above a certain value of V_E forward I_E begins to flow, increasing until the peak voltage V_P and current Ip are reached at point P.

After the peak point P an attempt to increase V_E is followed by sudden increases in emitter current I_E with decrease in V_E is a negative resistance portion of the curve.

The negative portion of the curve lasts until the valley point V is reached with valley point voltage Vv.and valley point current Iv after the valley point the device is driven to saturation the difference Vp-Vv is a measure of a switching efficiency of UJT fall of V_{BB} decreases

ADVANTAGES OF UJT

- It is a Low cost device
- It has excellent characteristics
- It is a low-power absorbing device under normal operating conditions

APPLICATIONS OF UJT

- It can be used as trigger device for SCR's and TRIAC's.
- To generate non sinusoidal oscillations.
- To generate saw tooth waveforms.
- In timing circuits it is used as switch.

SILICON CONTROLLED RECTIFIER (SCR)

The SCR is one of the most important semiconductor device in the industrial and power electronics field. The basic structure of SCR and its symbol is as shown in below figure.

Schematic Diagram
Symbolic Representation

Silicon Controlled Rectifier
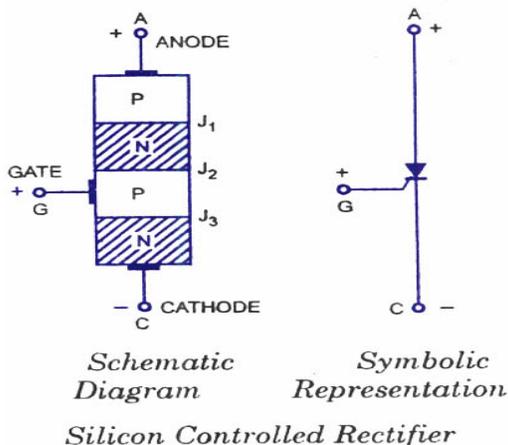
It consists of four semiconductor layers forming a p-n-p-n structure as shown in the above figure. It has three p-n junctions namely J_1, J_2 and J_3. There are three terminals called as anode (A), cathode (C) and gate (G) taken out. The gate terminal is joined to p-type layer near the lower end. Its symbol is shown in the above figure.

WORKING
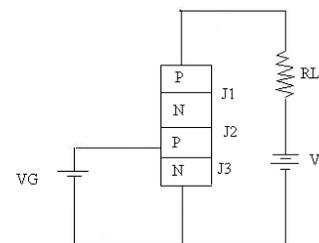
In SCR load is connected in series with anode. The anode is always kept at positive voltage with respect to cathode. The working can be discussed with the following points.

1. **When gate is open** – i.e. now voltage applied to the gate then J_2 is reverse biased while junctions J_1 and J_3 are forward biased. Hence no current flows through the load R_L as J_2 is reverse biased and SCR is set to be in off condition. If applied voltage is very high and reverse bias junction J_2 breaks down and SCR conducts heavily then it is said to be in on state. The applied voltage at which SCR conducts heavily without gate voltage is called break over voltage.

2. **When gate is positive with respect to cathode** – The SCR can be made to conduct heavily at smaller applied voltage by applying small positive voltage to the gate. Due to this all the three junctions are forward biased and current starts to flow through the device. The increased anode current makes more electrons available at junction J_2. This process continues and in extremely small time junction J_2 breaks down and SCR starts conducting heavily. Once SCR starts conducting heavily the gate loses all control, even if gate voltage is removed and anode current does not decease at all. The only way to stop conduction of SCR is to reduce applied voltage to zero.

TWO TRANSISTERIZED MODEL OF SCR

The equivalent circuit of SCR consists of pnp and npn transistor as shown in figure above. Collector of each transistor is coupled to the base of other transistor making positive feedback loop.

V – I CHARACTERISTICS OF SCR

V–I characteristics of the SCR with gate open.
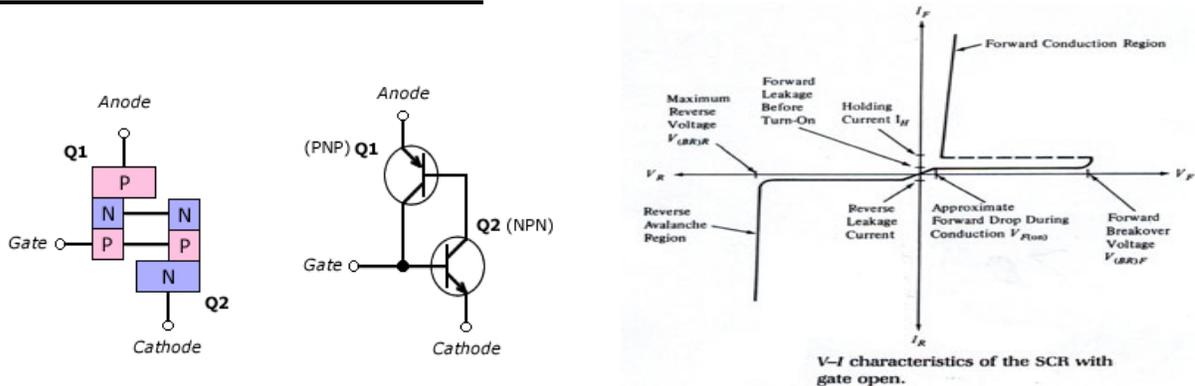
It is the curve between anode to cathode voltage (V_F) and anode current (I_F) of SCR at constant gate current.

1. **Forward characteristics** – When anode is positive with respect to cathode the curve between V_F and I_F is called the forward characteristics. The curve shown in the graph is the forward characteristics of SCR at $I_G=0$. If supply voltage is increased from zero a point is reached when SCR starts conducting. Under this condition the voltage across SCR suddenly drops as shown by dotted curve and most of supply voltage appears across the load R_L. Here I_H is holding current above which the SCR will be conducting. If proper gate current is made to flow, SCR can conduct at much smaller supply voltage.

2. **Reverse characteristics** – When anode is negative with respect to cathode the curve between V_R and I_R is known as reverse characteristics. If reverse voltage is gradually increased a small leakage current flows to the SCR. If we further increase reverse voltage, avalanche break down occurs and SCR start conducting heavily. This maximum reverse voltage at which SCR starts conducting heavily is known as a reverse break down voltage.

APPLICATIONS OF SCR
The SCR has no of applications as follows.
1. It is used for motor speed control.
2. Light dimming control.
3. Heater control
4. Phase control
5. Battery chargers
6. Inverters

7. Used as static switch
8. In power supply
9. In relay control

TRIAC:-

In thyrestor family, after SCR, TRIAC is the most widely used device for power control. The TRIAC is a bi-directional device with three terminals namely MT1, MT2 and gate. The gate is near the terminal MT1.

TRIAC is equivalent to two SCR connected in antiparallel. The symbolic representation and I-V characteristics of triac are shown in figure below:
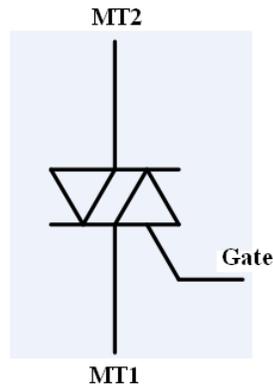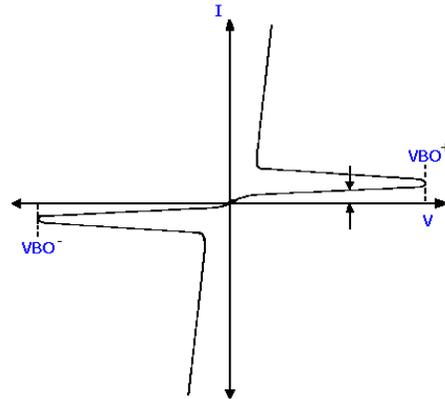

Fig.1 Symbol   Fig.2 Characteristic

When the gate is open the TRIAC will block both the polarities of the voltage applied across MT1 and MT2. If the magnitude of voltage is less than the breakover voltage of the device the characteristic of TRIAC are similar to those as SCR both in blocking and conducting state except for the fact that SCR conducts only in forward direction A to K, where as TRIAC conducts in both the direction. Because of this the terms anode and cathode are not used for TRIAC terminals. The TRIAC can be triggered into conduction by applying positive or negative to gate with respect to MT1, whereas SCR is triggered only by positive gate signal.